* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to the semiconductor substrate joining method to which semiconductor substrates are joined with the solder material which used the eutectic alloy.
[0002]
[Description of the Prior Art]Sending gas regularly in a gas passageway from a nozzle hole with a pump these days. The deflection status of the gas stream which flows through the inside of a gas passageway when angular velocity acts on a sensor body, As a gas rate sensor detected with the heat wire as a thermal resistance element of a couple installed by the deflection direction of the gas stream side by side in the gas passageway, That in which the sensor body portion which consists of a heat wire pair provided a gas passageway and in the gas passageway was formed by micro-machining processing of the semiconductor substrate using IC production technology is developed (refer to JP,3-29858,A).
[0003]As a sensor body in this kind of gas rate sensor, As shown in drawing 3 thru/or drawing 5, the half-hole 71 and the semisulcus 81 the bottom semiconductor substrate 5 and the upper part semiconductor substrate 6 which were formed by etching, It piles up so that each half-hole 71 and semisulcus 81 may be attached, and he is trying to constitute the nozzle hole 7 and the gas passageway 8 by joining both.
[0004]Among the figure, 91 and 92 are each heat wire provided in the gas passageway 8 at the couple, and pattern shaping is carried out at the upper surface of the bridge part 10 formed so that the bottom semiconductor substrate 5 might be etched and the gas passageway 8 might be started, respectively.
[0005]A deer is carried out, and in the gas rate sensor constituted in this way, when joining the bottom semiconductor substrate 5 and the upper part semiconductor substrate 6, while strengthening the junction, it is necessary to secure airtightness so that gas may not leak from the joined part.
[0006]It faces joining conventionally two semiconductor substrates by which micro-machining processing was carried out as art which joins a semiconductor substrate in order to constitute a pressure sensor, There is a thing to which heat to about 470 ** where two semiconductor substrates are piled up and pressurized, using glass as a solder material for making the junction perform with sufficient adhesion with airtightness firmly, and

it was made to join both (refer to JP,58-56476,A).

[0007]However, according to such a joining method, in particular when joining two semiconductor substrates which constitute a pressure sensor, it is satisfactory, but. When it is the gas rate sensor with which the thermal resistance element is allocated in the gas passageway and heats at an elevated temperature, using glass as a solder material for joining two semiconductor substrates, there is a problem that the characteristic of the thermal resistance element will be spoiled.

[0008]Although the anode joining art using Pyrex glass and Si direct junction art in which the oxidizing film was used are announced, high tension needs to be required or the plane of composition needs to be made into the pure mirror plane near an atom level for the formation of void free.

[0009]While forming a SiSn layer in the plane of composition of one semiconductor substrate 1 when joining two Si semiconductor substrates 1 and 2 as conventionally shown in drawing 7, He attains alloying with the SiSn layer and SiPd layer in the joining section of both the semiconductor substrates 1 and 2, and is trying to join both by heating, where a SiPd layer is formed and pressurized in the plane of composition of the semiconductor substrate 2 of another side.

[0010]However, in such a thing, while needing two kinds of things of SiSn and SiPd as a solder material, it is necessary to make the plane of composition of each semiconductor substrates 1 and 2 carry out the stratification of them, respectively, and complicated in respect of management of a solder material, and joining workability.

[0011]

[Problem(s) to be Solved by the Invention]When the problem which it is going to solve is joined by heating two substrates, applying a pressure using a solder material, It is having an adverse effect on the element which exists the neighborhood [a thermal resistance element allocated inside the gas passageway of the gas rate sensor formed by the cooking temperature of the solder material being high, for example, joining a semiconductor substrate].

[0012]When attaining alloying of a solder material and joining both by heating carrying out the stratification of the metal of a different kind to each plane of composition of two substrates as a solder material, respectively, and applying a pressure, it is that management of two kinds of solder materials and the workability of junction become complicated.

[0013]

[Means for Solving the Problem]So that this invention may have one kind of solder material and substrates can be joined with firmly and sufficient adhesion, So that cooking temperature of a solder material for junction may not have an adverse effect on an element allocated in the neighborhood and it can join with comparatively low cooking temperature, After applying an Au-Si system alloy used as hard solder to substrate junction and forming Au (gold) layer in at least one plane of composition of the two Si semiconductor substrates, He attains alloying with Si and Au in a joining section of both semiconductor substrates, and is trying to join both by heating in the state where it pressurized.

[0014]

[Example]If it is in the semiconductor substrate joining method by this invention, As shown in drawing 1, when joining two Si semiconductor substrates 1 and 2, an Au layer to the plane of composition of one semiconductor substrate 1 so that it may become a thickness of about 1 micrometer, After forming an Au layer in the plane of composition of the semiconductor substrate 2 of another side by vacuum evaporation, sputtering, or other means, respectively so that it may become a thickness of about 0.05 micrometer, Each of that plane of composition is attached where a certain amount of load is applied, it heats with conditions with an eutectic temperature of 370 ** so that Au will be 94% and Si may serve as 6% of alloy, and he attains alloying of a joining section, and is trying to join both.

[0015]In that case, it is effective to form an Au layer thinly so that the bias of a presentation may not be produced at the time of a heating alloy.

[0016]Heating is insufficient, and in order to avoid generating of the situation which becomes defecting joining, heating with which the temperature in a joining section becomes higher several 10 degrees than eutectic temperature is performed, and it is fully made to advance alloying as heating conditions. Specifically, heating of 1 hour is performed at 430 **, for example.

[0017]Since it will become a cause by which scaling of an adhesion side happens and an adhesive agent is started if it heats in the air, it is made to make it heat in nitrogen gas for antioxidizing.

[0018]When forming an Au layer in the plane of composition of each semiconductor substrates 1 and 2, in order to prevent carbon from the plane of composition oxidizing automatically, or being generated as an impurity, it is effective to make an Au layer form, immediately after an etching reagent washes the plane of composition of each semiconductor substrates 1 and 2.

[0019]If a 1-micrometer-thick Au layer is formed in one semiconductor substrate 1 side according to this invention, even if it will not form an Au layer in the semiconductor substrate 2 side of another side, alloying of the joining section of the semiconductor substrates 1 and 2 can be attained, and both can be joined.

[0020]As an Au-Si eutectic alloy, it excels in corrosion resistance or wettability electrochemically, and becomes what has high reliability, and becomes a hard alloy, and the joining section of the semiconductor substrates 1 and 2 becomes what has bond strength stable at below eutectic temperature and high.

[0021]What formed a 1-micrometer Au layer in the plane of composition of one semiconductor substrate 1, and formed a 0.05-micrometer Au layer in the plane of composition of the semiconductor substrate 2 of another side, respectively is attached now, When examined by pasting a jig and pulling the wafer which cut that to which both were joined by performing 430 ** heating in nitrogen gas for 1 hour to 6 mm squares, it is in the measurable ranges (not less than 10 kg) where adhesion with a jig does not peel, and peeling in the joining section was not seen.

[0022]when -30 degree and +85 degrees were examined by pulling moreover in every 10 100 times of thermal fatigue by the thermal shock using the same wafer, peeling of the joining section in measurable ranges was not seen.

[0023]Thus, while according to this invention being able to join the semiconductor substrates 3 and 4 now with sufficient adhesion firmly, using only Au as a solder material, a solder material's being one kind and the

management becoming easy, What is necessary is just to make an Au layer form at least in one side of the plane of composition of each semiconductor substrates 3 and 4, and the workability of junction improves.
[0024]Since eutectic alloy-ization of a joining section can be attained with comparatively low cooking temperature, what has a thermal adverse effect on the element which is allocated in the neighborhood, and which are allocated by the semiconductor substrate, for example, the heat wire in the main part of a gas rate sensor, etc., is controlled effectively.
[0025]As shown [this invention] in drawing 2, when the two substrates 3 and 4 consist of other than a Si semiconductor substrate, In order to raise adhesion to the plane of composition of each of those substrates 3 and 4, after forming in it the layer of the junction substrate which consists of titanium Ti at a thickness of about 0.1 micrometer, respectively, While forming an Au layer on junction substrate Ti of one substrate 3 at a thickness of about 1 micrometer, A Si layer is formed on junction substrate Ti of the substrate 4 of another side at a thickness of about 0.5 micrometer, and alloying with Si and Au in the joining section of both the substrates 3 and 4 is attained, and it is made to join both by heating from on the, further, where it formed the Au layer in a thickness of about 0.05 micrometer and it is pressurized.
[0026]Without providing an Au layer on the Si layer by the side of the substrate 4, even if it is in this case, the Au layer by the side of the substrate 3 and the Si layer by the side of the substrate 4 are attached directly, and it may be made to attain the alloying by heating of that joining section.
[0027]As a junction substrate for raising the adhesion of the substrates 3 and 4, nickel, platinum, etc. are used in addition to titanium Ti.
[0028]An example in the case of joining the bottom semiconductor substrate 5 and the upper part semiconductor substrate 6 in a sensor body of a gas rate sensor by this invention is shown in drawing 6.
[0029]Here, After forming in the prescribed spot of a Si substrate the mask pattern 11 which consists of SiN(s), using KOH solution by anisotropic etching. He is trying to form an Au layer about 1 micrometer thick via the layer of junction substrates, such as titanium Ti, on the mask pattern 11 in the plane of composition of the upper part semiconductor substrate 5 which carried out groove formation.
[0030]And after the etching process removed the mask pattern in the upper part semiconductor substrate 6 which carried out groove formation by anisotropic etching using KOH solution after forming in the prescribed spot of a Si substrate the mask pattern which consists of SiN(s) similarly and carrying out the denudation of the Si substrate, He is trying to form an Au layer about 0.05 micrometer thick in the plane of composition immediately after.
[0031]Thus, according to this invention, junction to the bottom semiconductor substrate 5 and the upper part semiconductor substrate 6 by which micro-machining processing was carried out can be made easily and to ensure using thin film coating technology now.
[0032]Since the heat wires 91 and 92 are formed in the bottom semiconductor substrate 5 as shown in drawing 4, Since there is a possibility that the heat wires 91 and 92 may be spoiled when the mask pattern in the bottom semiconductor substrate 5 is made to remove using an etching reagent, the mask pattern 11 of the bottom semiconductor substrate 5 is left intact.

[0033]

[Effect of the Invention]As mentioned above, if it is in the semiconductor substrate joining method by this invention, Junction of semiconductor substrates can be made to perform with thermal and chemical stability firmly using one kind of solder material Au, Eutectic alloy-ization of a joining section can be attained with comparatively low cooking temperature, and it has the advantage that what has a thermal adverse effect on the element allocated in the neighborhood can be controlled effectively.

[Translation done.]